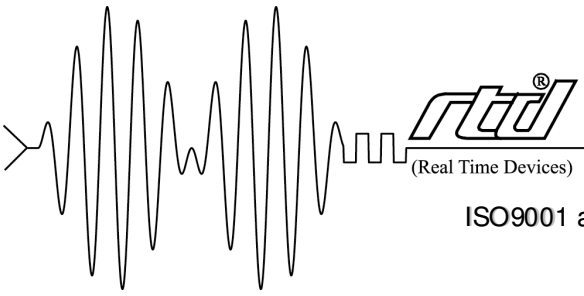
aAIO - Advanced Analog Input
Programming Manual



RTD Embedded Technologies, Inc.
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Rev. A

AAIO - ADVANCED ANALOG INPUT
Programming Manual

RTD Embedded Technologies, INC.
103 Innovation Blvd.
State College, PA 16803-0906

Phone: +1-814-234-8087
FAX: +1-814-234-5218

E-mail
sales@rtd.com
techsupport@rtd.com

web site
http://www.rtd.com

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1 INTRODUCTION

1.1 Purpose

This document presents the register interface to the Advanced Analog I/O (aAIO) functionality of RTD cpuModules. It is designed as a guide for developing the associated drivers and applications. This document also describes the hardware functionality of the board.

1.2 Features

- Eight single-ended or four differential analog inputs
- Up to 100kHz sample rate
- 16-bit resolution
- 0 to +5V, +/-5V, 0 to +10V, and +/-10V input ranges
    - Software configurable
- Per-channel digital filtering
- Per-channel threshold detection generates an interrupt when signal crosses high or low threshold.
- Advanced DMA
    - Each channel has it's own DMA buffer
    - Buffer chaining prevents interrupt latency problems
    - DMA to anywhere in 4GB address space

2 FUNCTIONAL DESCRIPTION

2.1 Block Diagram

The Figure below shows the functional block diagram of aAIO. The various parts of the block diagram are discussed in the following sections.

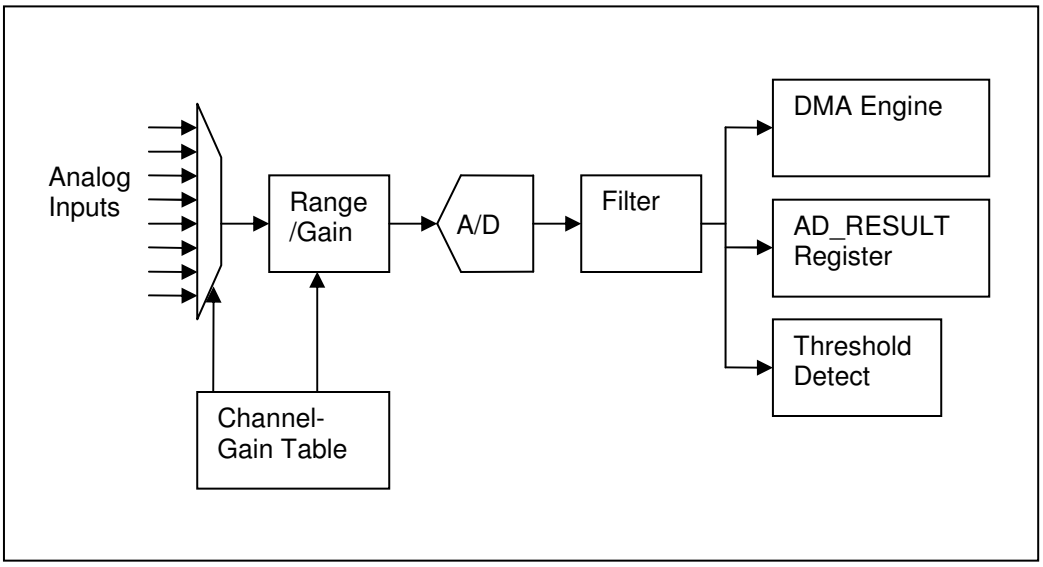

Figure 1: aAIO Block Diagram

2.2 Analog Inputs

The input multiplexer in aAIO accepts eight single ended analog inputs. Any combination of ranges can be used for these inputs. Pairs of analog inputs can be combined to form up to four differential inputs.

2.3 Channel-Gain Table

A Channel-Gain table is provided to control the mode and range of each channel and the order that they are sampled in. Each row in the scan table is associated with a specific A/D channel. When a scan is started (either by the pacer clock or a software trigger), channel 1 is sampled. Then the "NEXT_CHANNEL" pointer is followed to select the next channel to scan. The "NEXT_CHANNEL" pointer is followed until it is a value of 0, which ends the scan. There are a few implications:

1. The first channel to be scanned must always be Channel 1.
2. Each channel may only be sampled once per scan.
3. The scan list must end with a "NEXT_CHANNEL" of 0. Otherwise the channels will continue to scan without waiting for the pacer clock.

The Channel-Gain Table contains all of the channel-specific settings and status. This includes the mode (single-ended or differential), and range. It also contains the filter and threshold setting as well as the interrupt status and enable bits. The A/D Result register, which returns the last conversion for this channel, is also within the Channel-Gain Table.

2.4 Analog to Digital Converter

The Analog to Digital Converter used in aAIO is a 16-bit, 100 ksps converter. There is no calibration required, and is typically accurate to within 10mV.

2.5 Programmable Digital Filter

The programmable digital filter provides a single pole Infinite Impulse Response (IIR) filter on each channel. This is a unity-gain filter. The filtered data has a value of:

$$D_n = \frac{\left[D_{n-1} * \left(2^{ORDER} - 1\right)\right] + New\_Sample}{2^{ORDER}}$$

The response of the filter is shown in Figure 2 below. Table 1 below shows the -3 dB cutoff for each of the filter settings. Both the Figure and the Table are relative to the per-channel sample rate (f_s), which is:

$$f_s = \frac{40MHz}{\left(PACER\_DIVIDER - 1\right)}$$

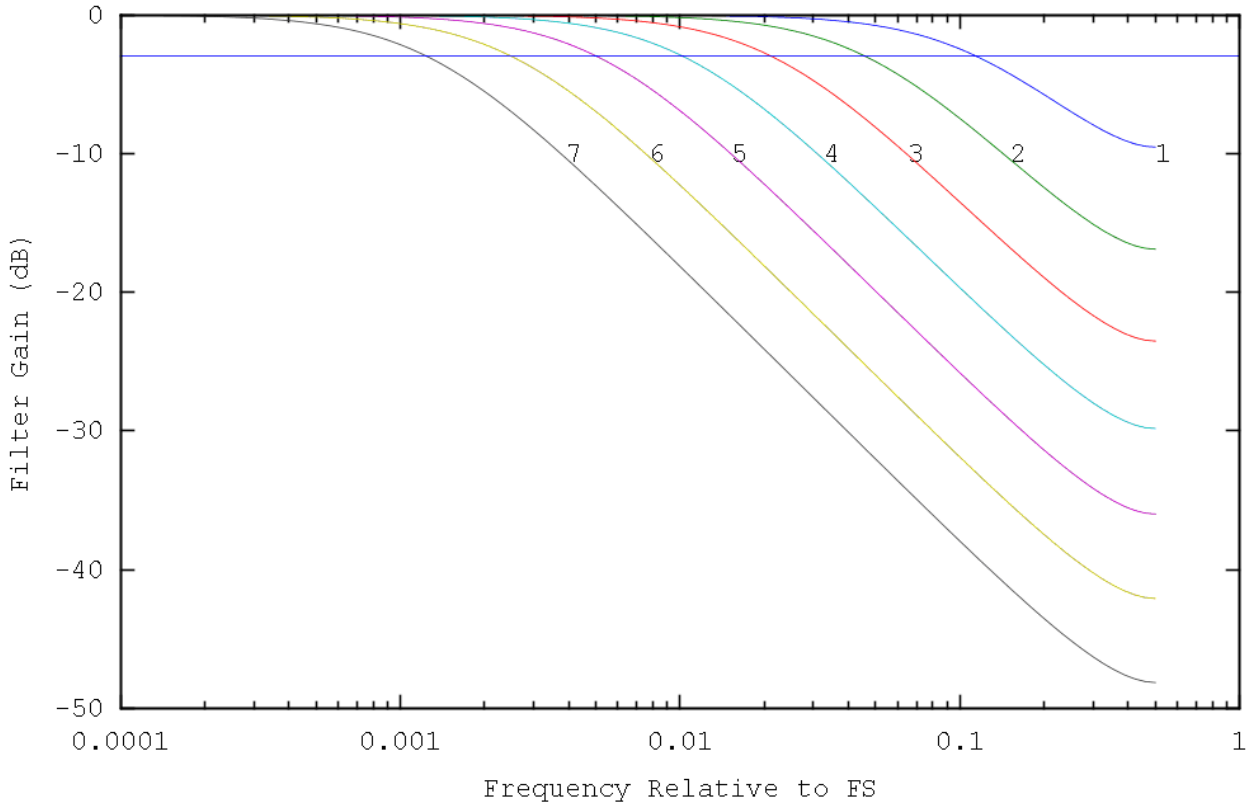

Figure 2: Filter Response with each ORDER Value

Table 1: Filter Cutoff Frequency

ORDER	-3 dB Cutoff
0	n/a
1	0.114791 * f_s
2	0.045995 * f_s
3	0.021236 * f_s
4	0.010255 * f_s
5	0.005042 * f_s
6	0.002501 * f_s
7	0.001246 * f_s

2.6 Threshold Detect

Threshold detection logic is provided to generate an interrupt when a channel crosses a high or low threshold. The thresholds can be individually set and monitored for each channel. Threshold crossings are only detected for a channel when that channel is sampled.

2.7 Data Output

2.7.1 Direct Read

The result from the most recent A/D conversion for a specific channel is always available in the AD_RESULT register within the scan table. The value returned is a 32-bit 2's complement value with same 76.294 microvolt resolution for all ranges.

2.7.2 DMA Engine

For data collection operations, a DMA engine is provided that will transfer the data results directly into system memory. This allows maximum data transfer rate with minimal interaction from the host software. In order to minimize the effects of interrupt latency, multiple DMA buffers can be defined in a Scatter-Gather Table.

2.7.2.1 Scatter-Gather Table

The DMA Engine contains a Scatter-Gather Table (SGT) for each of the eight inputs. The Scatter-Gather Table consists of a list of up to 64 entries. Each entry contains the physical address of a buffer that is 4kB in size, and 4kB aligned. It also contains a flag to indicate that the entry is valid. The Channel 1 Table also includes flags to stop DMA transfers, restart the SGT, or generate and interrupt. These are flags that effect all channels, and are only stored in the channel 1 table.

The DMA engine will transfer data using the same row of the SGT and the same offset for all channels. This guarantees that the captured data is synchronized. The DMA engine will always iterate through the SGT, even if DMA is not enabled for any channels.

The Scatter-Gather Table is not cleared at power up or during reset. Therefore, software must assume that it contains random, invalid data.

2.8 Operating Modes

2.8.1 Simple Operation

The simplest operating mode is using software to start the sampling and poll the aAIO for the result. This mode does not require setting up DMA buffers, or setting up the Scatter-Gather Table. In order to use this mode, perform the following steps:

1. Open the board as described in Section 4.1.
2. Write channel and input configuration in CGT Register if needed (default is +/-10V, single ended)
3. Do a software start conversion
4. Poll A/D done bit (about 20 microseconds) or wait for A/D Done interrupt
5. Read data from A/D Result

Alternately, the continuous sample bit can be set. In this case, the value read from the A/D Result register is the last captured sample.

2.8.2 DMA Based Operation

For higher performance sampling, a DMA engine is provided. This engine uses a scatter-gather table for each channel. The scatter-gather table can have up to 64 entries, each of which is a 4kB buffer that is 4kB aligned. At the completion of entry of the scatter-gather table, an interrupt can be generated, DMA transfers can be stopped, and/or the table can be restarted.

The scatter-gather DMA method allows continuous sampling at the maximum sample rate with the least amount of operating system intervention. Because each channel has its own scatter-gather table, the data for each channel is located in a separate area in system memory. Therefore the application software doesn't need to de-interlace the data.

The following steps are needed to use DMA operation:

1. Open the board as described in Section 4.1.
2. Allocate needed DMA buffers
3. Program Scatter-Gather table
4. Write channel and input configuration in CGT Register if needed (default is +/-10V, single ended)
5. Start conversion
6. Wait for DMA interrupt
7. Update Scatter-Gather table if needed
8. Process or move data if needed
9. Repeat to step #6

3 REGISTERS

3.1 Register Map

Table 2: aAIO Register Map

Name	I/O Port	31-24	23-16	15-8	7-0
Control	0x09E0	CH_IRQ_ENA	CH_IRQ_STAT	MODE_RESET	SELECT[3:0]
Pacer Clock Divider	0x09E4	PACER_DIVIDER			
Advanced Setup	0x09E8	Reserved	CUR_SGT_ROW	CUR_BUFFER_OFFSET	
Indexed registers controlled by 0x09E0[2:0]					
Channel Control	0x09EC	FILTER_CON	SGT_ROW	CH_MODE	NEXT_ CHANNEL
A/D Result	0x09F0	AD_RESULT			
Interrupt	0x09F4		IRQ_ENA		IRQ_STAT
Threshold	0x09F8	THRESH_HIGH		THRESH_LOW	
DMA Buffer	0x09FC	SGT_DATA			

3.2 Detailed Register Description

3.2.1 Control Registers

3.2.1.1 0x9E0: SELECT

Table 3: SELECT Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R	R	R	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Field	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	CGT_Channel		

CGT_Channel Selects the channel to be displayed in the Channel Gain Table Registers. See Section 3.2.2.

3.2.1.2 0x9E1: MODE_RESET

Table 4: MODE_RESET Register

Bit	7	6	5	4	3	2	1	0
Mode	R/W	R/W	W	W	R/W	R/W	R/W	R/WC
Default	0	0	0	0	0	0	0	1
Field	Rsvd	Rsvd	Clear	Reset	Rsvd	Rsvd	GO	SW_Trig

SW_Trig Write a '1' to generate a trigger to scan through the Channel Gain Table regardless of the state of the "Go" bit. Will read '0' while the scan is happening, and '1' when completed.

GO Set to '1' to begin continuous sampling based on the Pacer Clock.

Reset Write '1' to reset all aAIO registers, including the "Clear" functions. Always reads '0'.

Clear Write '1' to stop sampling, clear the Filters, and reset the Scatter-Gather and DMA Offset counters. Always reads '0'.

3.2.1.3 0x9E2: CH_IRQ_STAT

Table 5: CH_IRQ_STAT Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R	R	R	R	R	R
Default	0	0	0	0	0	0	0	0
Field	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

Chx A '1' indicates that an interrupt is pending from channel 'x' of the Channel Gain Table. This bit is set regardless of CH_IRQ_ENA. This is a non-stick register, and will be cleared when the interrupt condition is cleared in the Channel Gain Table.

3.2.1.4 0x9E3: CH_IRQ_ENA

Table 6: CH_IRQ_ENA Register

Bit	7	6	5	4	3	2	1	0
Mode	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default	0	0	0	0	0	0	0	0
Field	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1

Chx Writing a '1' enabled generation of an interrupt when the same bit of the CH_IRQ_STAT register goes high.

3.2.1.5 0x9E4: PACER_DIVIDER

Read-only during sampling

Table 7: PACER_DIVIDER Register

Bit	31	0
Mode	R/W	
Default	0x00000000	
Field	PACER_DIVIDER	

PACER_DIVIDER A 32-bit divider for the pacer clock. When the pacer clock rolls over, the Channel Gain Table is scanned at a rate of 100kHz. This register should only be modified when sampling is stopped. The time between scans is:

$$Scan\_Rate = \frac{40MHz}{(PACER\_DIVIDER + 1)}$$

The maximum sample rate is 100kHz. The maximum scan rate is 100kHz divided by the number of channels scanned. Any PACER_DIVIDER value that would yield a sample rate of greater than 100kHz has undefined results, except a PACER_DIVIDER value of 0x00000000 will sample at the fastest rate possible.

3.2.1.6 0x9E8: CUR_BUFFER_OFFSET

Table 8: CH_IRQ_ENA Register

Bit	16 12	11 0
Mode	R	R
Default	0	0
Field	Reserved	CUR_BUFFER_OFFSET

CUR_BUFFER_OFFSET The offset into the current 4kB DMA buffer where data will be written next. This is the same value for every channel, i.e. the channels are always synchronized.

3.2.1.7 0x9EA: CUR_SGT_ROW

Table 9: CH_IRQ_ENA Register

Bit	7	6	5	4	3	2	1	0
Mode	R		R					
Default	0		0					
Field	Reserved		CUR_SGT_ROW					

CUR_SGT_ROW The current row in the Scatter-Gather Table that will be used for the next transfer. This is the same value for every channel, i.e. the channels are always synchronized.

3.2.2 Channel Gain Table Registers

The registers described in this section are paged based on the value of SELECT[CGT_CHANNEL] in Section 3.2.1.1. These can be though of as rows in a scan table, each associated with a specific A/D channel. When a scan is started (either by the pacer clock or a software trigger), channel 1 is sampled. Then the "NEXT_CHANNEL" pointer is followed to select the next channel to scan. The "NEXT_CHANNEL" pointer is followed until it is a value of 0, which ends the scan. There are a few implications:

4. The first channel to be scanned must always be Channel 1.
5. Each channel may only be sampled once per scan.
6. The scan list must end with a "NEXT_CHANNEL" of 0. Otherwise the channels will continue to scan without waiting for the pacer clock.

The channel associations for CGT_CHANNEL and NEXT_CHANNEL are shown below.

Table 10: Channel Gain Table Channels

CGT_CHANNEL/ NEXT_CHANNEL Value	Single Ended	Differential
0	Channel 1 (Pin 1)	Ch1(+), Ch2(-)
1	Channel 2 (Pin 2)	Ch2(+), Ch1(-)
2	Channel 3 (Pin 3)	Ch3(+), Ch4(-)
3	Channel 4 (Pin 4)	Ch4(+), Ch3(-)
4	Channel 5 (Pin 5)	Ch5(+), Ch6(-)
5	Channel 6 (Pin 6)	Ch6(+), Ch5(-)
6	Channel 7 (Pin 7)	Ch7(+), Ch8(-)
7	Channel 8 (Pin 8)	Ch8(+), Ch7(-)

3.2.2.1 0x9EC: NEXT_CHANNEL

Read-only during sampling

Table 11: NEXT_CHANNEL Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R	R	R	R/W		
Default	0	0	0	0	0	(Channel + 1)		
Field	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	NEXT_CHANNEL		

NEXT_CHANNEL The next channel to sample in the Channel Gain Table.

3.2.2.2 0x9ED: CH_MODE

Read-only during sampling

Table 12: CH_MODE Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R/W	R/W	R	R/W		
Default	0	0	0	0	0	101		
Field	Rsvd	Rsvd	DMA	Rsvd	Rsvd	RANGE		

RANGE Selects the range of this channel, and differential/single ended as show below.

Table 13: Channel Mode

Value	SE/DIFF	Range
0 (000)	DIFF	±5V
1 (001)	DIFF	±10V
2 (010)	DIFF	0 to 5V
3 (011)	DIFF	0 to 10V
4 (100)	SE	±5V
5 (101)	SE	±10V
6 (110)	SE	0 to 5V
7 (111)	SE	0 to 10V

DMA Set to '1' to enable DMA. Data will be moved to the DMA buffer as soon as it is available.

3.2.2.3 0x9EE: SGT_ROW

Table 14: SGT_ROW Register

Bit	7	6	5	4	3	2	1	0
Mode	R		R/W					
Default	0		0					
Field	Reserved		SGT_ROW					

SGT_ROW The row in the Scatter-Gather Table that is visible and can be modified by the SGT_DATA register at 0x9FC.

3.2.2.4 0x9EF: FILTER_CON

Table 15: FILTER_CON Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R	R	R	R/W		
Default	0	0	0	0	0	0		
Field	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	ORDER		

ORDER Selects the order of the filter for this channel. A value of "000" disables the filter. The filtered data has a value of.

$$D_n = \frac{\left[D_{n-1} * \left(2^{ORDER} - 1\right)\right] + New\_Sample}{2^{ORDER}}$$

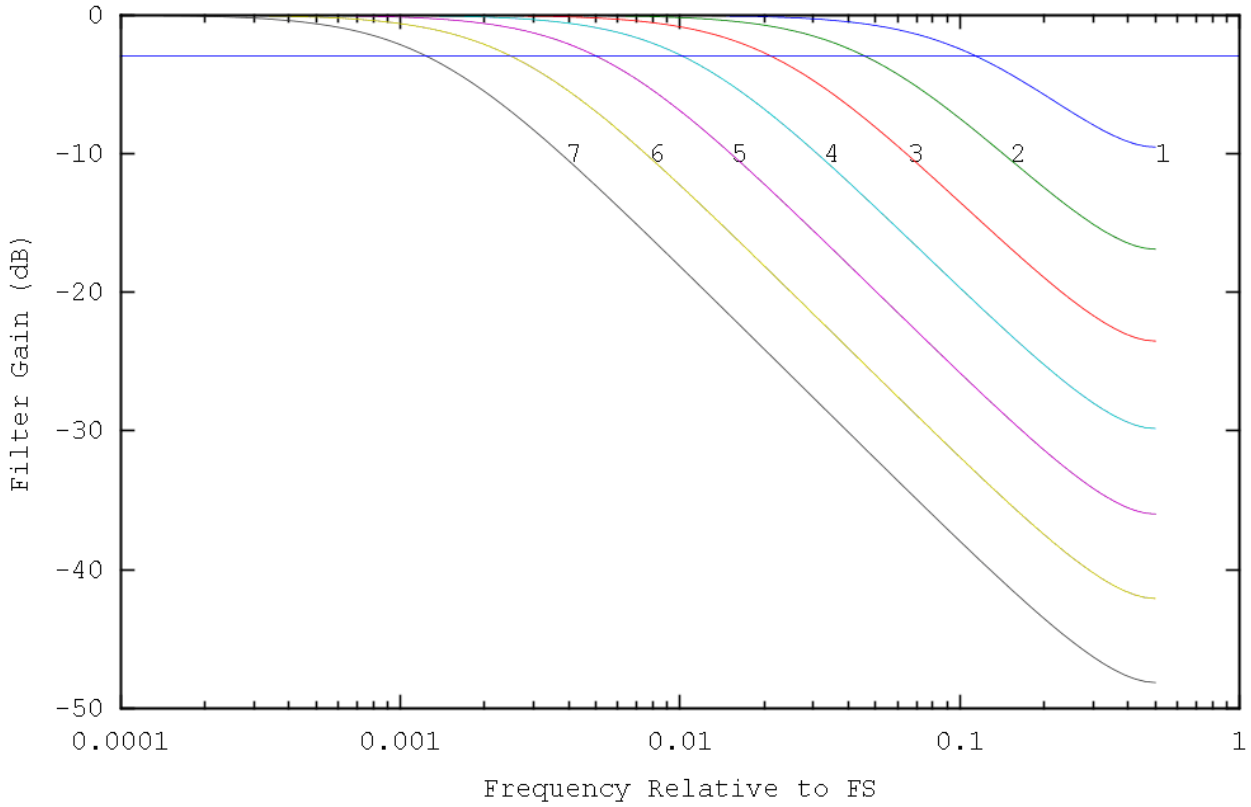

Figure 3: Filter Response with each ORDER Value

Table 16: Filter Cutoff Frequency

ORDER	-3 dB Cutoff
0	n/a
1	0.114791 * f_s
2	0.045995 * f_s
3	0.021236 * f_s
4	0.010255 * f_s
5	0.005042 * f_s
6	0.002501 * f_s
7	0.001246 * f_s

f_s = 40 MHz / (PACER_DIVIDER – 1)

3.2.2.5 0x9F0: AD_RESULT

Table 17: AD_RESULT Register

Bit	31	0
Mode	R	
Default	0x00000000	
Field	AD_RESULT	

AD_RESULT The current value of the A/D converter for this channel after filtering. This is a 32-bit 2's complement value with same 76.294 microvolt resolution for all ranges.
0 to +5V range – A/D data is converted to 2's complement
0 to +10V range – A/D data is converted to 2's complement and shifted left one position
-5 to +5V range – A/D data shifted left one position
-10 to +10V range – A/D data shifted left two positions

Range/Bits	31-18	17	16	15-2	1	0
0 to +5V	0	0	0	Straight Binary A/D Data		
0 to +10V	0	0	Straight Binary A/D Data			0
-5 to +5V	Sign Extend	Sign Extend	2's Complement A/D Data			0
-10 to +10V	Sign Extend	2's Complement A/D Data			0	0

3.2.2.6 0x9F4: IRQ_STAT

Table 18: IRQ_STAT Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R/C	R/C	R/C	R/C	R	R/C
Default	0	0	0	0	0	0	0	0
Field	Rsvd	Rsvd	Thresh High	Thresh Low	DMA Error	DMA	Rsvd	Sample

A '1' indicated the condition exists, regardless of IRQ_ENA. Write a '1' to clear.

Sample A sample has been converted.

DMA An SGT row with the IRQ bit set has been filled.

DMA Error DMA for this channel didn't get serviced in time (gap in data).

Thresh Low Channel is below the low threshold.

Thresh High Channel is above the high threshold.

3.2.2.7 0x9F6: IRQ_ENA

Table 19: IRQ_ENA Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R/W	R/W	R/W	R/W	R	R/W
Default	0	0	0	0	0	0	0	0
Field	Rsvd	Rsvd	Thresh High	Thresh Low	DMA Error	DMA	Rsvd	Sample

A '1' allows in interrupt to be generated if the corresponding bit in IRQ_STAT is set.

Sample A sample has been converted.

DMA An SGT row with the IRQ bit set has been filled.

DMA Error DMA for this channel didn't get serviced in time (gap in data).

Thresh Low Channel is below the low threshold.

Thresh High Channel is above the high threshold.

3.2.2.8 0x9F8: THRESH_LOW

Table 20: THRESH_LOW Register

Bit	16	0
Mode	R/W	
Default	0x8000	
Field	THRESH_LOW	

THRESH_LOW This register sets the low threshold for this channel. It contains a 16-bit 2's complement value with the same 305.175 microvolt resolution (20V / 65536) for all ranges. The high threshold must be greater than low threshold. The default for low threshold is the maximum negative value. If the A/D reading for this channel is less than the low threshold, the IRQ_STAT[Thresh Low] bit is set.

3.2.2.9 0x9FA: THRESH_HIGH

Table 21: THRESH_HIGH Register

Bit	16	0
Mode	R/W	
Default	0x7FFF	
Field	THRESH_HIGH	

THRESH_HIGH This register sets the high threshold for this channel. It contains a 16-bit 2's complement value with the same 305.175 microvolt resolution (20V / 65536) for all ranges. The high threshold must be greater than low threshold. The default for the high threshold is the maximum positive value. If the A/D reading for this channel is greater than the high threshold, the IRQ_STAT[Thresh High] bit is set.

3.2.2.10 0x9FC: SGT_DATA

This register is used to view and modify the data in the Scatter-Gather Table. It is indexed both by SELECT[CGT_Channel] (to select the channel), and SGT_ROW (to select the row in the table).

The Scatter-Gather Table consists of a list of up to 64 entries. Each entry contains the physical address of a buffer that is 4kB in size, and 4kB aligned. It also contains a flag to indicate that the entry is valid. The Channel 1 Table also includes flags to stop DMA transfers, restart the SGT, or generate and interrupt. These are flags that effect all channels, and are only stored in the channel 1 table.

The DMA engine will transfer data using the same row of the SGT and the same offset for all channels. This guarantees that the captured data is synchronized. The DMA engine will always iterate through the SGT, even if DMA is not enabled for any channels.

The Scatter-Gather Table is not cleared at power up or during reset. Therefore, software must assume that it contains random, invalid data.

Table 22: DMA_BUFFER Register

Bit	31 12	11 9	8	7	6	5	4 0
Mode	R/W	R	R/W	R/W	R/W	R/W	R
Default	X	X	X	X	X	X	00000
Field	ADDRESS	Rsvd	IRQ	STOP	RESTART	VALID	Rsvd

ADDRESS The upper 20-bits of a DMA buffer 4k in size and 4k aligned. The DMA data will start at an offset of 0 into the buffer. After it is full, the DMA engine will advance to the next row in the table based on the flags.

IRQ Flag to generate and interrupt after this buffer is full. The interrupt will be generated for all channels that DMA is enabled on. This flag is only checked for Channel 1.

STOP Flag to stop DMA on all channels after this buffer is full. This flag is only checked for Channel 1.

RESTART Flag to restart the SGT at row 0 after this buffer is full. This flag should always be set for the last entry in the table, even if the STOP flag is also set. This flag is only checked for Channel 1.

VALID Flag to indicate that this is a valid entry. DMA data will only be transferred if the VALID flag is set. This flag is checked for all channels.

3.2.3 BIOS Setup Register

This register is for the BIOS to enable aAIO and set the interrupt

3.2.3.1 0x9CE: aAIO_SETUP

Table 23: aAIO_SETUP Register

Bit	7	6	5	4	3	2	1	0
Mode	R	R	R	R	R/W	R/W		
Default	0	0	0	0	0	0		
Field	Rsvd	Rsvd	Rsvd	Rsvd	ENA	IRQ		

ENA Set to '1' to enable aAIO.

IRQ Set the IRQ:
000 = Disabled
001 = IRQ5
010 = IRQ7
011 = IRQ10
100 = IRQ11
101 = IRQ12
110 = IRQ3
111 = IRQ6

4 USAGE NOTES

4.1 Board Open

If the shift register that controls the A/D is reset in the middle of a transfer, the next sample that you try to get may be bad. The only time that this problem could happen is if the system is reset (CTRL+ALT+DEL, etc.) in the middle of sampling. However, the following procedure will ensure that correct data will be available for the first sample.

1. Perform a Board Reset to make sure all the registers are default
2. Do a software triggered sample
3. Wait for it to be done
4. Perform a Board Reset to reset the sample counter.

4.2 Changing Ranges

The channel ranges are only actually updated during sampling. If, for example, you are sampling a 3V signal in the 0-5V range, then stop sampling, connect a 9V signal, and start sampling in the 0-10V range, the input to the A/D will be over-driven. The A/D requires approximately 150us to recover from an over-driven condition. When changing ranges, be sure to start sampling before applying a signal that would be outside of the previous range.

5 GETTING TECHNICAL SUPPORT

For help with this product, or any other product made by RTD, you can contact RTD Embedded Technologies via the following methods:

- Phone: +1-814-234-8087
- E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

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USA
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