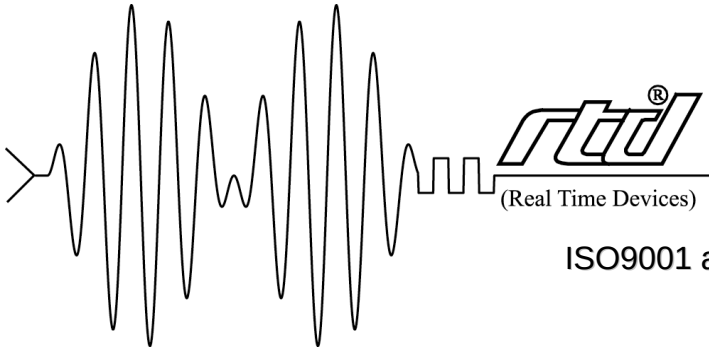
BRG17088HR User's Manual

PCI to ISA Bridge PC/104-Plus Module



RTD Embedded Technologies, Inc.

(Real Time Devices)

"Accessing the Analog World"®

ISO9001 and AS9100 Certified

BDM-610020053
Rev D

BRG17088HR User's Manual

RTD EMBEDDED TECHNOLOGIES, INC.
103 Innovation Blvd
State College, PA 16803-0906

Phone: +1-814-234-8087
FAX: +1-814-234-5218

E-mail
sales@rtd.com
techsupport@rtd.com

Web Site
http://www.rtd.com

Manual Revision History

Rev A	Initial Release (Preliminary)
Rev B	Documented jumperless operation
Rev C	Changed references of PORT1 and PORT2 to PORT0 and PORT1.
Rev D	Added notes for “-M” version (for use with Montevina)

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RTD Embedded Technologies, Inc.
103 Innovation Boulevard
State College, PA 16803

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Introduction

Product Overview

The BRG17088HR is designed to provide a PCI to ISA interface for RTD's Pentium M and Celeron M family PCI-104 cpuModules.

Board Features

- PCI to ISA Bridge
  - Allows legacy ISA-based PC/104 modules to work with modern PCI-104 CPUs while maintaining software transparency
  - Subtractive decode of all ISA addresses
  - Full ISA bus support
    - I/O and memory-mapped devices
    - 8-bit and 16-bit cycles
    - All ISA IRQ lines
    - All ISA DMA channels (except –M version)
    - ISA Bus Masters
  - Does not support ISA IDE or floppy controllers or ISA video cards
- Digital I/O
  - ISA bus advanced digital I/O (aDIO)
  - 8 bit-programmable with individual pull-up/down resistors
  - 8 port programmable with individual pull-up/down resistors
  - 2 strobes with individual pull-up/down resistors
  - Match, event and strobe interrupts
  - Address and interrupt selection in CPU BIOS
  - PC/104-*Plus* compliant
  - Universal (3.3V or 5.0V) PCI Signaling

I/O Interfaces

- 40-pin DIL digital I/O connectors
  - 0.1" Pin Spacing
  - Can be cabled directly to a 37-pin "D" connector
- PC/104-*Plus* (PCI) stack-through bus connector
- PC/104 (ISA) stack-through bus connector

Getting Technical Support

If you are having problems with your system, please try the following troubleshooting steps:

- **Simplify the System** – Remove modules one at a time from your system to see if there is a specific module that is causing a problem.
- **Swap Components** – Try replacing parts in the system one-at-a-time with similar parts to determine if a part is faulty or if a type of part is configured incorrectly.

If problems persist, or you have questions about configuring this product, obtain the PCI BIOS listing information of the BRG17088HR and other modules in the system. After you have this information, contact RTD Embedded Technologies via the following methods:

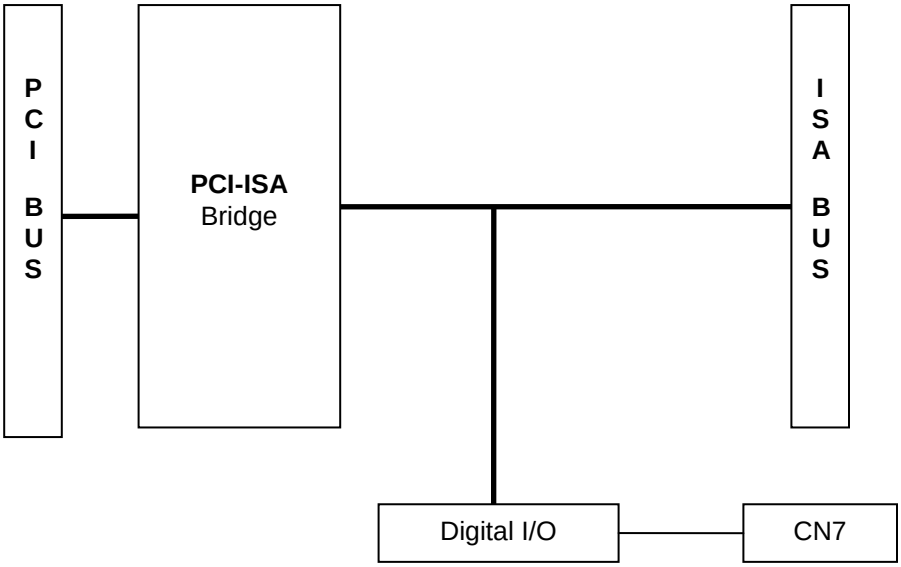
Phone: +1-814-234-8087

E-Mail: techsupport@rtd.com

Be sure to check the RTD web site (http://www.rtd.com) frequently for product updates, including newer versions of the board manual and application software.

Hardware Description

Below is a block diagram of the BRG17088HR.

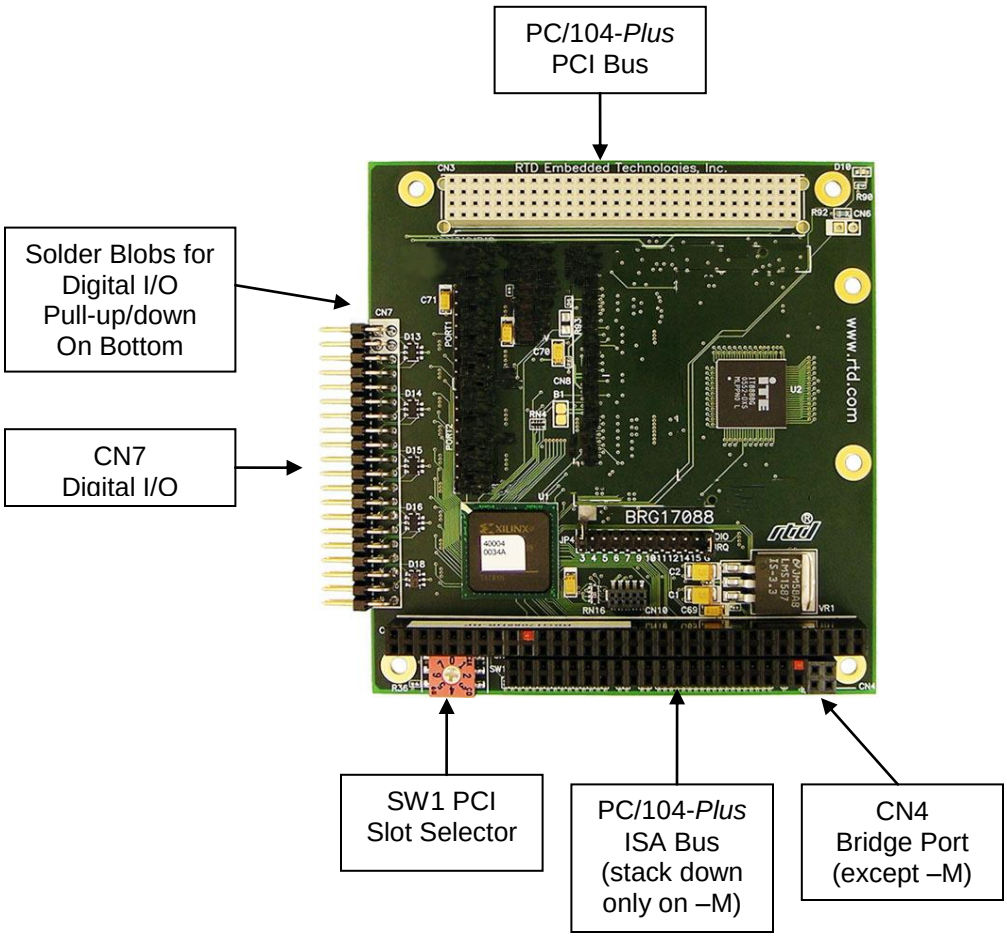


Board Connections

Connector and Jumper Locations

The following diagram shows the location of all connectors and jumpers on the BRG17088HR. Future revisions of the BRG17088HR may have cosmetic differences. For a description of each jumper and connector, refer to the following sections.

BRG17088HR Connector and Jumper Locations



External I/O Connections

The following sections describe the external I/O connections of the BRG17088HR.

Bridge Port, CN4

Four pin connector for communication with RTD's Pentium M and Celeron M cpuModules.

CN4 is not populated on the "-M" version for use with Montevina cpuModules.

Advanced Digital Input/Output, CN7

Pin 1 is indicated by a square solder pad.

Table 1: Advanced Digital I/O Connector Pinout CN7

CN7 Pin	Function	DB37
1	P0-0	1
2	Gnd	20
3	P0-1	2
4	Gnd	21
5	P0-2	3
6	Gnd	22
7	P0-3	4
8	Gnd	23
9	P0-4	5
10	Gnd	24
11	P0-5	6
12	Gnd	25
13	P0-6	7
14	Gnd	26
15	P0-7	8
16	Gnd	27
17	P0-Strobe	9
18	Gnd	28
19	P1-0	10
20	Gnd	29
21	P1-1	11
22	Gnd	30
23	P1-2	12
24	Gnd	31
25	P1-3	13
26	Gnd	32
27	P1-4	14
28	Gnd	33
29	P1-5	15
30	Gnd	34
31	P1-6	16
32	Gnd	35
33	P1-7	17
34	Gnd	36
35	P1-Strobe	18
36	Gnd	37
37	+5 Volts Fused @ 2A	19
38	Gnd	N/C
39	Gnd	N/C
40	Gnd	N/C

Jumpers

The following sections describe the jumper configuration options available on the BRG17088HR. For a reference that shows the location of each set of jumpers, refer to the diagram of the BRG17088HR at the beginning of this chapter.

B1 – B8 & B17 aDIO Port 0, Pull High/Low (Default = Open)

These solder blobs allow the user to pull individual bits of digital I/O port 0 on CN7 to a TTL high or low through a 10K ohm resistor.

Port 1 Bits 0-7	Function and Default Setting
P0-0 (CN7-1)	B1 1-2 = High, 2-3 = Low, Default = Not Connected
P0-1 (CN7-3)	B2 1-2 = High, 2-3 = Low, Default = Not Connected
P0-2 (CN7-5)	B3 1-2 = High, 2-3 = Low, Default = Not Connected
P0-3 (CN7-7)	B4 1-2 = High, 2-3 = Low, Default = Not Connected
P0-4 (CN7-9)	B5 1-2 = High, 2-3 = Low, Default = Not Connected
P0-5 (CN7-11)	B6 1-2 = High, 2-3 = Low, Default = Not Connected
P0-6 (CN7-13)	B7 1-2 = High, 2-3 = Low, Default = Not Connected
P0-7 (CN7-15)	B8 1-2 = High, 2-3 = Low, Default = Not Connected
P0-Strobe (CN7-17)	B17 1-2 = High, 2-3 = Low, Default = Not Connected

B9 – B16 & B18 aDIO Port 1, Pull High/Low (Default = Open)

These solder blobs allow the user to pull individual bits of digital I/O port 1 on CN7 to a TTL high or low through a 10K ohm resistor.

Port 2 Bits 0-7	Function and Default Setting
P1-0 (CN7-19)	B9 1-2 = High, 2-3 = Low, Default = Not Connected
P1-1 (CN7-21)	B10 1-2 = High, 2-3 = Low, Default = Not Connected
P1-2 (CN7-23)	B11 1-2 = High, 2-3 = Low, Default = Not Connected
P1-3 (CN7-25)	B12 1-2 = High, 2-3 = Low, Default = Not Connected
P1-4 (CN7-27)	B13 1-2 = High, 2-3 = Low, Default = Not Connected
P1-5 (CN7-29)	B14 1-2 = High, 2-3 = Low, Default = Not Connected
P1-6 (CN7-31)	B15 1-2 = High, 2-3 = Low, Default = Not Connected
P1-7 (CN7-33)	B16 1-2 = High, 2-3 = Low, Default = Not Connected
P1-Strobe (CN7-35)	B18 1-2 = High, 2-3 = Low, Default = Not Connected

aDIO Base Address Selection (Default = disabled)

Note: Board revision AA used jumpers for the selection of the base address for aDIO use. Refer to manual BDM-610020053 Rev A for information on the jumper usage. This manual is available from RTD Embedded Technologies, Inc. Technical Support.

The aDIO requires four (4) consecutive I/O address starting at a base address. There is an option in RTD's Pentium M or Celeron M BIOS to select the Bridge Board aDIO base address. This is located under ADVANCED / Miscellaneous RTD Features / ISA Bridge DIO Base Address. Any software that accesses the board will do so through reads and writes to the I/O address set by the BIOS. To function properly, the I/O address the software is expecting must match the base address set by the BIOS.

When selecting a base address for the BRG17088, please observe the following guidelines:

- Every device in your system must have a unique address range!
- When selecting a base address for the BRG17088, make certain that it does not conflict with any other devices.

aDIO Interrupt Selection (Default = none)

Note: Board revision AA used jumpers for the selection of the IRQ for aDIO use. Refer to manual BDM-610020053 Rev A for information on the jumper usage. This manual is available from RTD Embedded Technologies, Inc. Technical Support.

There is an option in RTD's Pentium M or Celeron M BIOS to select the Bridge Board aDIO interrupt. This is located under ADVANCED / Miscellaneous RTD Features / ISA Bridge DIO IRQ.

PCI Board Selector, SW1

Since the utilityModule™ uses stack through buses, the only hardware installation you will need to do is to place the module onto the PC/104-*Plus* or PCI-104 stack. To do this, you will connect the PCI and/or ISA bus connectors on the CM17407HR to the respective connectors of your stack.

The BRG17088 uses a rotary switch to select the PCI slot. Before you can use this module you have to set the PCI board selector switch. The procedure is if this module is the first module from the CPU module select '0,' if it is the second module select '1,' etc. Positions 4 - 7 are simply repeats of positions 0 – 3.

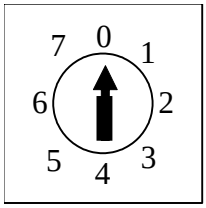


Figure 1: PCI Selector Rotary Switch PCI Board Selector

Board Installation

Installing the Hardware

The BRG17088HR can be installed into a PC/104-*Plus* or PCI-104 stack. It can be located almost anywhere in the stack, above or below the CPU as long as all PCI bus constraints are met and the Bridge Port connector can be connected to the CPU.

Static Precautions

Keep your board in its antistatic bag until you are ready to install it into your system! When removing it from the bag, hold the board at the edges, and do not touch the components or connectors. Handle the board in an antistatic environment, and use a grounded workbench for testing and handling of your hardware.

Steps for Installing

1. Shut down the PC/104-*Plus* system and unplug the power cord.
2. Ground yourself with an anti-static strap.
3. Set the PCI Slot Selector as described in the previous chapter.
4. If any other PCI add-on cards are to be included in the stack, be sure that their PCI slot numbers are configured correctly (Slot 0 for the board closest to the CPU, Slot 1 for the next board, etc).
5. Line up the pins of the BRG17088's PC/104 and PC/104-*Plus* connectors with the corresponding bus connectors of the stack. Make sure that both connectors are lined up.
6. Apply pressure to both bus connectors and gently press the board onto the stack. The board should slide into the matching bus connectors. Do not attempt to force the board, as this can lead to bent/broken pins.
7. Connect the Serial IRQ and Serial DMA lines (CN4) to the appropriate connection on the CPU. In some RTD configuration this connector may stack directly to the CPU.
8. If any boards are to be stacked above the BRG17088, install them.
9. Attach any necessary cables to the PC/104-*Plus* stack.
10. Re-connect the power cord and apply power to the stack.
11. Boot the system and verify that all of the hardware is working properly.

Note: If multiple PCI devices are configured to use the same PCI slot number, the system may not boot.

System Configuration

Reserving IRQ and DMA Channels

At boot time, the BIOS of the CPU allocates IRQs and DMA channels for PCI devices. Since the ISA bus does not support the ability to detect used IRQs and DMA channels, it is possible for a PCI device to claim resources which you intend to use for one of the installed ISA boards. If this happens, there will be a resource conflict, which will prevent both boards from working.

To prevent this, most BIOSes support the ability to reserve IRQ and DMA resources for the ISA bus. When a resource is reserved, a PCI device will not claim it.

If you are using an ISA board that requires an IRQ or DMA channel, it is strongly recommended that you reserve all necessary resources in the BIOS setup before installing the board into your system.

Compatibility Concerns

While the BRG17088 can physically support almost any PC/104 ISA board, some types of ISA boards require special BIOS initialization at boot time. These boards include:

- Video Controllers
- IDE Controllers
- Floppy Controllers

Since the ISA bus is a legacy technology, many modern BIOSes have removed support for the boards listed above. If these boards are not supported by the CPU's BIOS, you will be unable to use them in your system. If you intend to use one of the boards listed above in your system, contact your CPU vendor to verify compatibility.

aDIO Programming

This board supports 16 bits of TTL/CMOS compatible digital I/O (TTL signaling) plus two strobe inputs. These I/O lines are grouped into two ports, port 0 and port 1. Port 0 is bit direction programmable and Port 1 is byte programmable. At power-up all digital I/O line are programmed as inputs.

The aDIO registers are I/O mapped. Their location in I/O space is determined by the CPU BIOS settings.

aDIO Register Descriptions

Offset from Base Address	Register Name
0	Port 0 Data
1	Port 1 Data
2	Multi-Function
3	DIO-Control

Port 0 Data I/O address aDIO_Base + 0

D7	D6	D5	D4	D3	D2	D1	D0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Port 0 Data register is a read/write bit direction programmable register. A particular bit can be set to input or output. A read of an input bit returns the value of port 0. A read of an output bit returns the last value written to Port 0. A write to an output bit sends that value to port zero.

Port 1 Data I/O address aDIO_Base + 1

D7	D6	D5	D4	D3	D2	D1	D0
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Port 1 Data register is a read/write byte direction programmable register. A read on this register when it is programmed to input will read the value at the DIO connector. A write on this register when it is programmed as output will write the value to the DIO connector. A read on this register when it is set to output will read the last value sent to the DIO connector.

Multi-Function I/O address aDIO_Base + 2

D7	D6	D5	D4	D3	D2	D1	D0

The Multi-Function register is a read/write register whose contents are set by the DIO-Control register. See the DIO-Control register description for a description of this register.

DIO-Control I/O address aDIO_Base + 3 Read Access

D7	D6	D5	D4	D3	D2	D1	D0
Strobe0 Status	Digital IRQ Status	Strobe1 Status	Digital IRQ Mode		Port 1 Direction	Multi-Function Register Select	
0 = no strobe 1 = strobe	0 = no digital interrupt 1 = digital interrupt	0 = no strobe 1 = strobe	00 = Disabled 01 = Strobe 10 = Event 11 = Match		0 = Input 1 = Output	00 = Clear Mode 01 = Port 0 Direction 10 = Mask Register 11 = Compare Register	

Clear Register:

A read to this register clears the IRQs and a write to this register sets the DIO-Compare, DIO-Mask, DIO-Control, Port1 and Port0 to zeros. A write to this register is used to clear the board.

Port 0 Direction Register:

Writing a zero to a bit in this register makes the corresponding pin in the DIO connector an input. Writing a one to a bit in this register makes the corresponding pin in the DIO connector an output.

Mask Register:

Writing a zero to a bit in this register will not mask off the corresponding bit in the DIO-Compare register. Writing a one to a bit in this register masks off the corresponding bit in the DIO-Compare register. When all bits are masked off the DIOs comparator is disabled. This condition means Event and Match mode will not generate an interrupt. This register is used by Event and Match modes.

Compare Register:

A Read/Write register used for Match Mode. Bit values in this register that are not masked off are compared against the value on Port 0. A match or Event causes bit 6 of DIO-Control to be set and if the DIO is in Advanced interrupt mode, the Match or Event causes an interrupt.

DIO-Control I/O address aDIO_Base + 3 Write Access

D7	D6	D5	D4	D3	D2	D1	D0
Reserved			Digital IRQ Mode		Port 1 Direction	Multi-Function Register Select	
			00 = Disabled 01 = Strobe 10 = Event 11 = Match		0 = Input 1 = Output	00 = Clear Mode 01 = Port 0 Direction 10 = Mask Register 11 = Compare Register	

Advanced Digital Interrupts

The Digital I/O can use interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15. To use any of the listed interrupts set the interrupt aside for an ISA legacy device in the CPU BIOS setup.

There are three advanced digital interrupt modes available. These three modes are Event, Match, and Strobe. The use of these three modes is to monitor state changes at the DIO connector. The three modes are selected with bits D[4:3] of the DIO-Control Register.

Event Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. There is a deglitching circuit inside the DIO circuitry. The deglitching requires pulses on Port 0 to be at least 120 nanoseconds in width. As long as changes are present longer than that, the event is guaranteed to register. Pulses as small as 60 nanoseconds can register as an event but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Event mode, set bits D[4:3] of the DIO-Control register to a “10”.

Match Mode

When this mode is enabled, Port 0 is latched into the DIO-Compare register at 8.33 MHz. There is a deglitching circuit inside the DIO circuitry. The deglitching requires pulses on Port 0 to be at least 120 nanoseconds in width. As long as changes are present longer than that, the match is guaranteed to register. Pulses as small as 60 nanoseconds can register as a match but they must occur between the rising and falling edge of the 8.33 MHz clock. To enter Match mode, set bits D[4:3] of the DIO Control register to “11”.

> **Note: Make sure bit 3 is set BEFORE writing the DIO-Compare register. If you do not set bit 3 first, the contents of the DIO-Compare register could be lost. The reason for this is that Event mode latches in Port 0 into the DIO-Compare register at an 8.33 MHz rate.**

Strobe Mode

Strobe Mode allows the strobe pin of the DIO connector to trigger an interrupt. A low to high transition on the strobe pin will cause an interrupt request. The request will remain high until the Clear Register is read from. Additionally, the Compare Register latched in the value at Port 0 when the Strobe pin made a low to high transition. No further strobes will be available until a read of the Compare Register is made. What this implies is one must read the Compare Register then clear interrupts so that the latched value in the compare register is not lost. To enter Strobe mode, set bits D[4:3] of the DIO-Control register to “01”.

For More Information

For more information about interrupts and writing interrupt service routines, refer to the following book:

Interrupt-Driven PC System Design
by Joseph McGivern
ISBN: 0929392507

BRG17088HR Specifications

Physical Attributes

Size:	3.6”L x 3.8”W x 0.6”H (90mm L x 96mm W x 15mm H)
Weight:	0.24bs (0.10 Kg)
Power Consumption:	1W @ 5 VDC Typical

Operating Conditions

Cooling	Convection
Operating temperature range	-40º to +75ºC (+85 on request)
Storage temperature range	-55° C to +125° C
Humidity	RH up to 95% non-condensing

Limited Warranty

RTD Embedded Technologies, Inc. warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from RTD EMBEDDED TECHNOLOGIES, INC. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, RTD EMBEDDED TECHNOLOGIES will repair or replace, at its option, any defective products or parts at no additional charge, provided that the product is returned, shipping prepaid, to RTD EMBEDDED TECHNOLOGIES. All replaced parts and products become the property of RTD EMBEDDED TECHNOLOGIES. Before returning any product for repair, customers are required to contact the factory for an RMA number.

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